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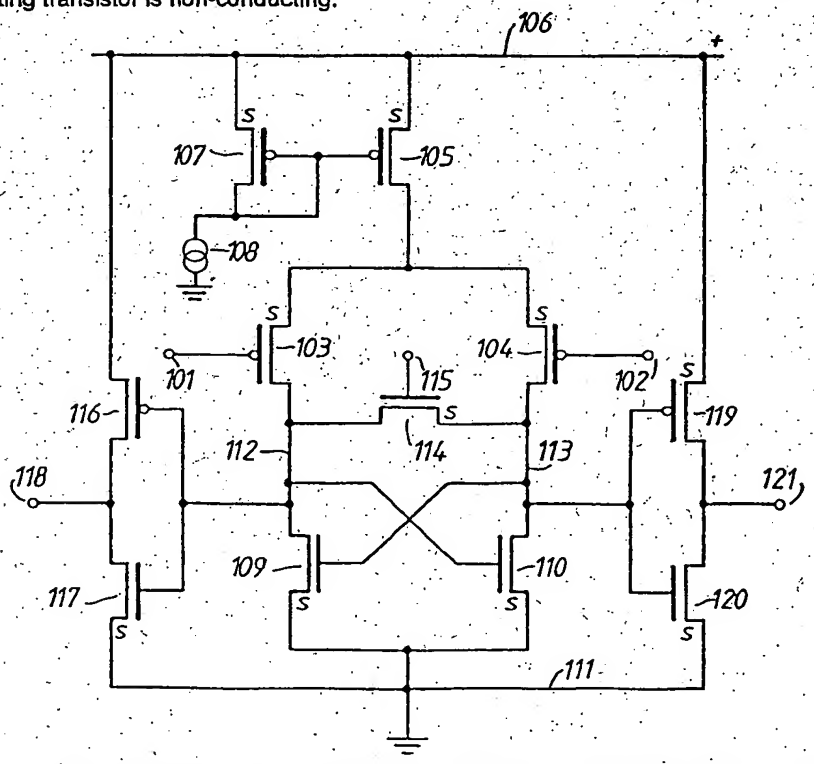
(54) A comparator circuit

(57) A switched comparator is described for deriving binary values from an input signal. The comparator consists of a long-tailed pair of MOS transistors with the input signal and a threshold value signal respectively applied to the gates, and a cross-coupled pair connected drain-to-drain to the long-tailed pair, with the output taken from one of the commoned drain connections. A gating MOS transistor is connected between the commoned drain connections so that an output is obtained only when the gating transistor is non-conducting.



The date of filing shown above is that provisionally accorded to the application in accordance with the provisions of Section 15(4) of the Patents Act 1977 and is subject to ratification or amendment.

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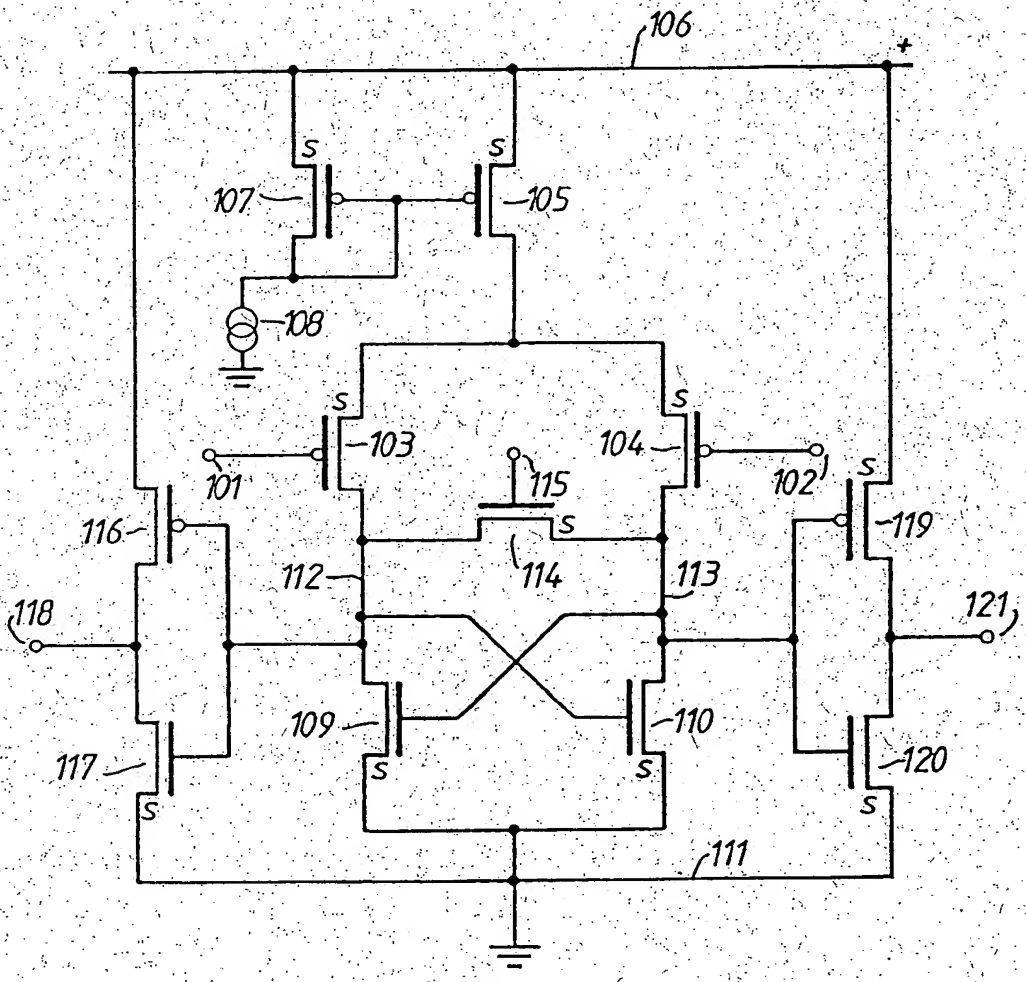
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IMPROVEMENTS IN OR RELATING TO COMPARATOR CIRCUITS

This invention relates to comparator circuits.

It is an object of the present invention to provide an improved comparator circuit.

According to an aspect of the invention there is provided a comparator circuit for producing an output signal indicating which of two input signals has the higher voltage at a given instant, the circuit including a first pair of MOS transistors of a first conductivity type connected as a long-tailed pair and to the gates of which the input signals are respectively applied, a second pair of MOS transistors of a second conductivity type opposite to the first conductivity type, connected as a cross-coupled pair and with their drains connected respectively to the drains of the first pair of MOS transistors, the output signal being obtained from one or other or both of the commoned drain connections, and a normally conducting fifth MOS transistor having its source-drain path connected between the commoned drain connections of the pairs of MOS transistors and its gate connected to receive a gating signal defining the given instant by assuming for that instant a voltage capable of causing the fifth MOS transistor to be non-conducting.

An example of a comparator circuit in accordance with the invention will now be described with reference to the single figure of the accompanying drawing which shows a circuit diagram of a clocked comparator circuit for comparing a received signal with a threshold level at particular instants in time.

The clocked comparator described herein is suitable for use in the digital signal processor hat is described in the copending Application No. 88.22114.8, Publication No. 2 225 198, entitled "Improvements in or relating to Digital Signal Processors", filed by Texas Instruments Limited, from which this application is divided. That digital

signal processor receives a video signal containing teletext data and separates out the teletext data. In that digital signal processor the clocked comparator described herein is used to sample the video signal at a rate of 55.5 MHz. However it is to be understood that the clocked comparator is not limited in its usefulness to sampling the level of a teletext signal but can be used to compare any two signals.

The Figure shows the circuit of an example of the clocked comparator. In the Figure, the signals to be compared are applied via terminals 101 and 102 respectively to the gates of p-channel MOSFET's 103 and 104 connected as a long-tailed pair. The tail of the long-tailed pair is a current source formed by a p-channel MOSFET 105 having its source connected to a positive supply conductor 106. The gate of the MOSFET 105 is connected to the gate and drain of another p-channel MOSFET 107 of which the source is connected to the conductor 106. A current source 108 feeds current to the drain of the MOSFET 107, the MOSFET's 105 and 107 forming a current mirror. The current source 108 may be simply a high value resistor connected to ground, but since in some applications, for example, the digital signal processor mentioned above, the comparator is part of a large integrated circuit the current source may be formed by current mirror means supplying controlled currents to other parts of the circuit and connected to an external resistor.

The drains of the MOSFET's 103 and 104 are connected to the drains of a cross-coupled pair of n-channel MOSFET's 109 and 110, the sources of which are connected to a grounded conductor 111. The cross-coupling of the MOSET's 109 and 110 is formed in each case by a direct connection from the drain of one transistor to the gate of the other. The commoned drain connections 11 and 113 are interconnected by the source-drain path of an n-channel MOSFET 114, the gate of which is connected to a terminal 115. The

commoned drain connection 112 is connected through a CMOS inverter circuit formed by the MOSFET's 116 and 117 to an output terminal 118. The connection 113 is connected through a CMOS inverter circuit formed by the MOSFET's 119 and 120 to a terminal 121. The output from the comparator may be taken from either or both of the connections 112 and 113 or from the terminal 118 or 121.

In the operation of the comparator shown in the Figure, the input signals are applied via the terminals 101 and 102, and unless the input signals are of very similar voltage one of the MOSFET's 103 and 104 will be rendered conducting and the other non-conducting, because their sources are maintained at the same potential by the tail of the long-tailed pair. If the voltage of the input signals are similar the transistors 103 and 104 will operate as a differential amplifier so that the amplified difference voltage tends to appear between the drains of the MOSFET's. Initially, the MOSFET 114 is conducting because a positive voltage is applied to the terminal 115, and therefore the connections 112 and 113 are maintained at the same potential. At this time the output voltage or voltages derived from one or other or both of the connections 112 and 113 are the same and do not depend on the input voltages but are set by the current supplied by the MOSFET 105. When the voltage applied to the terminal 115 goes negative, the MOSFET 114 ceases to conduct, so that the drain of one of the MOSFET's 103 and 104 tends to go more positive than that of the other and this difference in voltage rapidly causes the cross-coupled pair of MOSFET's 109 and 110 to bring the voltage of one of the connections 112 and 113 to be close to ground potential and the other to move towards the positive supply potential. Under these circumstances, the voltages on the connections 112 and 113 differ, and which is high and which is low is determined by the relative magnitudes of the voltages applied to the input terminals 101 and 102.

When it is required to reset the comparator a positive voltage is again applied to the terminal 115 causing the MOSFET 114 to conduct again. This rapidly brings the potentials of the connections 112 and 113 to the same value depending entirely on the current supplied by the MOSFET 105. This method of resetting the comparator enables a cross-coupled pair of MOSFET's to be used for the comparison, such a circuit having a very high speed of response to voltage differences by virtue of the regenerative feedback. The disadvantage of a cross-coupled pair that they introduce hysteresis into the comparison is avoided by the use of the short-circuiting MOSFET 114 to reset the comparator; this MOSFET holds the drain voltages of the cross-coupled pair to the same voltages overriding the regenerative feedback. The short-circuiting MOSFET 114 also permits the long-tailed pair of MOSFET's 103 and 104 to establish their conductive states in response to the input signal without hysteresis before the comparator is clocked to produce an output signal.

Since the voltages on the connections 112 and 113 whilst the MOSFET is conducting are dependent on the current supplied by the MOSFET 105, the threshold voltage of conduction of the MOSFET 115 is constant and independent of the input voltages. This means that the sampling of the input signals is carried out at a precise time, that is to say, when the clock voltage falls below the gate threshold voltage of the MOSFET 114.

It will be appreciated that because of the symmetry there is no systematic offset voltage to interfere with the comparison of the two input voltages.

When a clocked comparator is used in the digital signal processor mentioned above, the clocking frequency is 55.5 MHz and it has been found that a 10 mV difference between the input signals applied to the comparator can cause the production of appropriate 0 and 1 outputs after 3 ns.

CLAIMS:

1. A comparator circuit for producing an output signal indicating which of two input signals has the higher voltage at a given instant in time, the circuit including a first pair of MOS transistors of a first conductivity type connected as a long-tailed pair and to the gates of which the input signals are respectively applied, a second pair of MOS transistors of a second conductivity type opposite to the first conductivity type, connected as a cross-coupled pair and with their drains connected respectively to the drains of the first pair of MOS transistors, the output signal being obtained from one or other or both of the commoned drain connections, and a normally conducting fifth MOS transistor having its source-drain path connected between the commoned drain connections of the pairs of MOS transistors and its gate connected to receive a gating signal defining the given instant in time by assuming for that instant a voltage capable of causing the fifth MOS transistor to be non-conducting.

2. A comparator circuit according to claim 1, wherein the sources of the MOS transistors of the first pair are connected to a constant current source.

3. A comparator circuit according to claim 1 or claim 2, wherein the gate of each of the MOS transistors of the second pair is directly connected to the drain of the other MOS transistors of that pair.

4. A comparator substantially as described herein and as illustrated by the single Figure of the accompanying drawing.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

(i) UK Cl (Edition K) H3P PPXX

(ii) Int Cl (Edition 5) H03K 3/356 5/22

Search Examiner
S J DAVIES

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search
16 OCTOBER 1992

Documents considered relevant following a search in respect of claims 1-4

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	US 4511810 (YUKAWA) column 5, line 45 - column 6, line 10	1-4

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

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